



# HubRouter: Learning Global Routing via Hub Generation and Pin-hub Connection

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# Introduction



## Global Routing



Chip Canvas and Netlist



#### Grid Graph

# Introduction

## Existing works



BoxRouter



DRL









## **(e)** the disconnectivity of PRNet



Original route Generated route

Metric	Case	PRNet (GAN)
Correctness Rate (%)	Route-small-4Route-smallRoute-large-4Route-large	0.806 0.334 0.196 0.040

the disconnectivity proportion



# Methodology



## Route and hubs

**Definition 1** (**Hub**). Given a one-channel image with  $m \times n$  pixels, let  $p_{ij}$   $(1 \le i \le m, 1 \le j \le n)$ denote the pixel in the *i*-th row and *j*-th column, whose value  $r_{ij} = 1/0$  respectively represent routed/unrouted. Auxiliary denote  $r_{0j} = r_{(m+1)j} = r_{i0} = r_{i(n+1)} = 0$ , then the pixel  $p_{ij}$  is a hub if and only if  $r_{ij} = 1$  and it satisfies any of the following condition:

$$(1) + :r_{(i-1)j} = r_{(i+1)j} = r_{i(j-1)} = r_{i(j+1)} = 1; \quad (2) + :r_{(i-1)j} + r_{i(j+1)j} + r_{i(j-1)} + r_{i(j+1)} = 3; \quad (3) \sqcup :r_{(i-1)j} + r_{(i+1)j} = 1 \text{ and } r_{i(j-1)} + r_{i(j+1)} = 1; \quad (4) \cdot :r_{(i-1)j} + r_{(i+1)j} + r_{i(j-1)} + r_{i(j+1)} = 1.$$







#### **Two-phase learning framework**







#### Correctness rate, wirelength rate, and generation time on ISPD-07

Metric Case		PRNetHubRouter(GAN)(VAE)		HubRouter (DPM)	HubRouter (GAN)	
Correctness Rate (%)	Route-small-4 Route-small Route-large-4 Route-large	0.806 0.334 0.196 0.040	$\begin{array}{c} 1.000 \pm 0.000 \\ 1.000 \pm 0.000 \\ 1.000 \pm 0.000 \\ 1.000 \pm 0.000 \end{array}$	$\begin{array}{c} 1.000 \pm 0.000 \\ 1.000 \pm 0.000 \\ 1.000 \pm 0.000 \\ 1.000 \pm 0.000 \end{array}$	$\begin{array}{c} 1.000 {\pm} 0.000 \\ 1.000 {\pm} 0.000 \\ 1.000 {\pm} 0.000 \\ 1.000 {\pm} 0.000 \end{array}$	
Wirelength Rate (%)	Route-small-4 Route-small Route-large-4 * Route-large *	<b>1.001</b> 1.009 - -	$\begin{array}{c} 1.099 {\scriptstyle \pm 0.020} \\ 1.042 {\scriptstyle \pm 0.006} \\ 1.122 {\scriptstyle \pm 0.039} \\ 1.041 {\scriptstyle \pm 0.014} \end{array}$	$\begin{array}{c} 1.060 \pm 0.011 \\ 1.174 \pm 0.009 \\ 1.100 \pm 0.021 \\ 1.242 \pm 0.021 \end{array}$	$\begin{array}{c} 1.011 {\scriptstyle \pm 0.003} \\ \textbf{1.002 } {\scriptstyle \pm 0.001} \\ \textbf{1.005 } {\scriptstyle \pm 0.002} \\ \textbf{1.001 } {\scriptstyle \pm 0.000} \end{array}$	
Generation Time (GPU Sec)	Route-small-4 Route-small Route-large-4 Route-large	14.99 18.51 19.47 19.22	$\begin{array}{c} \textbf{7.14}{\scriptstyle\pm 0.19} \\ \textbf{7.70}{\scriptstyle\pm 0.20} \\ \textbf{7.24}{\scriptstyle\pm 0.30} \\ \textbf{10.65}{\scriptstyle\pm 0.09} \end{array}$	$\begin{array}{r} 673.21{\scriptstyle\pm 5.08}\\ 670.23{\scriptstyle\pm 2.45}\\ 673.01{\scriptstyle\pm 5.18}\\ 672.86{\scriptstyle\pm 4.44}\end{array}$	$\begin{array}{c} 7.16 {\scriptstyle \pm 0.05} \\ 8.36 {\scriptstyle \pm 0.35} \\ 7.53 {\scriptstyle \pm 0.16} \\ \textbf{9.75} {\scriptstyle \pm \textbf{0.35}} \end{array}$	





## **Wirelength and inference time on ISPD-98**

Metric	Model	IBM01	IBM02	IBM03	IBM04	IBM05	IBM06	GRL-8	<b>GRL-16</b>
WL	Labyrinth 24	75909	201286	187345	195856	420581	341618	2376	8204
	Boxrouter 8	63687	172304	147463	169033	410614	280477	2328	7991
	DQN 30	OOT	OOT	OOT	OOT	OOT	OOT	2434	8356
	PRNet 6	61950	172802	152037	170493	420274	287777	2497	8172
	HR-VAE	64703±1498	$176492 \pm 6830$	159968±3281	$179895 \pm 5274$	434942±2916	300448±5560	2415±33	8584±244
	HR-DPM	66446±1586	190588±2337	$168454 \pm 2486$	183696±1736	475820±5516	316700±2843	2285±7	7746±29
	HR-GAN	61056±151	$167545{\scriptstyle\pm236}$	$147050{\scriptstyle\pm208}$	$164298{\scriptstyle\pm326}$	411857±472	$278198{\scriptstyle\pm423}$	2306±8	7768±30
Time (Sec)	Labyrinth 24	6.47	10.14	12.07	36.81	7.54	18.43	< 1 second	< 1 second
	Boxrouter 8	7.01	12.91	11.74	41.76	13.45	29.17	< 1 second	< 1 second
	DQN 30	OOT	OOT	OOT	OOT	OOT	OOT	> 1 day	> 1 day
	PRNet 6	254.31	585.23	523.34	573.19	1606.00	1227.31	11.54	28.25
	HR-VAE	$9.66 \pm 0.08$	9.69±0.04	$10.19{\scriptstyle \pm 0.06}$	$12.93{\scriptstyle \pm 0.07}$	$14.58 \pm 0.00$	$17.28 \pm 0.16$	$5.83 \pm 0.01$	$5.88 \pm 0.02$
	HR-DPM	1796.09±38.68	2772.29±16.83	2936.52±21.23	3865.21±25.07	4369.47±22.56	$4965.08 \pm 121.46$	$37.00 \pm 2.58$	53.90±2.85
	HR-GAN	41.02±0.51	$46.58{\scriptstyle \pm 0.56}$	52.04±2.35	67.31±3.51	72.28±3.72	88.02±4.45	$6.31 \pm 0.20$	$6.38 \pm 0.04$

# Limitation



The two-phase scheme is not end-to-end under a joint training scheme;

- The supervised module for hub generation depends on large amount of training data;
- The further decrease on overflow needs a reroute process;
- Finally, it would also be compelling to integrate the learning-based methods of logic synthesis, with routing methodologies, including those presented in this work. This would allow for a data-driven approach to the chip design pipeline.



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Thank you



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